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Substitute for form 1449A/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(use as many sheets as necessary)</i>		Complete if Known	
		Application Number	09/899,977
		Filing Date	6 July 2001
		First Named Inventor	Keeth, et al
		Group Art Unit	2848 2827
		Examiner Name	Not Yet Assigned M. TRAN
		Attorney Docket Number	DB000575-015
Sheet	1	of	1

[illegible][illegible]

Examiner Signature	/Michael Tran/	Date Considered	06/15/2007
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¹ Unique citation designation number. ² See attached Kinds of U.S. Patent Documents. ³ Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). ⁴ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. ⁶ Applicant is to place a check mark here if English language Translation is attached.

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Subtitle for form 1449A/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)			Complete if Known	
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			Filing Date	July 6, 2001
			First Named Inventor	Keeth et al.
			Group Art Unit	Not yet assigned 2827
			Examiner Name	Not yet assigned M. TRAIN
Sheet 1 of 3			Attorney Docket Number	DB000575-015

U.S. PATENT DOCUMENTS						
Examiner Initials*	Cite No.†	U.S. Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appert
		Number	Kind Code‡ (If known)			
/MT/		6,043,118		Suwanai et al.	03/28/2000	
		5,960,455		Bauman	09/28/1999	
		5,838,627		Tomishima et al.	11/17/1998	
		5,677,645		Merritt	10/14/1997	
		5,651,011		Keeth	07/22/1997	
		5,614,859		Ong	03/25/1997	
		5,574,697		Manning	11/12/1996	
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		5,552,739		Keeth et al.	09/03/1996	
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		5,231,605		Lee	07/27/1993	
		5,212,440		Waller	05/18/1993	
		5,159,273		Wright et al.	10/27/1992	
		5,155,704		Walther et al.	10/13/1992	
/MT/		4,970,725		McEntroe et al.	11/13/1990	

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PAGE 66/68 * RCVD AT 8/23/2004 2:11:33 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-3/26 * DNIS:2731795 * CSID: * DURATION (mm:ss):18:16 * Burden Hour Statement: This form is estimated to take 20 hours to complete. * Case: Any comments on this case should be directed to the assigned examiner at the address below. * Office, Washington, DC 20231.

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Sheet 2 of 3

Complete if Known

Application Number	Not yet assigned	09/899977
Filing Date	July 6, 2001	
First Named Inventor	Keeth et al.	
Group Art Unit	Not yet assigned	2827
Examiner Name	Not yet assigned	M. TRAN
Attorney Docket Number	DB000575-015	

OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.*	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume/issue number(s), publisher, city and/or country where published.	T*
/MT/		SUGIBAYASHI ET AL., "A 30-ns 256-Mb DRAM with a Multidivided Array Structure", IEEE Journal of Solid-State Circuits, Vol. 28 (No. 11), (November 1993)	
		TAGUCHI ET AL., "A 40-ns 64-Mb DRAM with 64-b Parallel Data Bus Architecture", IEEE Journal of Solid-State Circuits, Vol. 28 (No. 11), (November 1991)	
		KITSUKAWA ET AL., "256-Mb DRAM Circuit Technologies for File Applications", IEEE Journal of Solid-State Circuits, Vol. 28 (No. 11), (November 1993)	
		JEDEC SOLID STATE PRODUCTS ENGINEERING COUNCIL, "Committee Letter Ballot", JC-42.3-95-73, Item #633.13, Arlington, VA (April 1995)	
		YOO ET AL., "6P 23.6: A 32-Bank 1Gb DRAM with 1 GB/s Bandwidth", ISSCC96/Session 23/DRAM/PAPER SP 23.6	
		NIITA ET AL., "SP 23.5: A 1.6GB/s Data-Rate 1Gb Synchronous DRAM with Hierarchical Square-Shaped Memory Block and Distributed Bank Architecture", ISSCC96/Session 23/DRAM PAPER SP 23.5	
		U.S. Patent Application S.N. 08/521,563, entitled IMPROVED VOLTAGE REGULATOR CIRCUIT, filed 8/30/95	
		U.S. Patent Application S.N. 08/688,347, entitled DIFFERENTIAL VOLTAGE REGULATOR, filed 8/26/96	
		U.S. Patent Application S.N. 08/460,234, entitled SINGLE DEPOSITION LAYER METAL DYNAMIC RANDOM ACCESS MEMORY, filed 8/17/95	
		U.S. Patent Application S.N. 08/420,943, entitled DYNAMIC RANDOM-ACCESS MEMORY, filed 6/4/95	
/MT/		U.S. Patent Application S.N. 08/194,184, entitled INTEGRATED CIRCUIT POWER SUPPLY HAVING PIECEWISE LINEARITY, filed 2/8/94	

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